| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/966,316 | MIS ET AL. | |
| | Examiner | Art Unit | |
| | William C. Vesperman | 2813 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *1/22/2004*.

2. ☒ The allowed claim(s) is/are *2-17,19-28,63-68,70-73 and 76-81*.

3. ☒ The drawings filed on *27 September 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 6/30/2003
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

## DETAILED ACTION

1. This application is in response to applicant's amendment of 1/22/2004.

### *Response to Amendment*

2. The affidavits filed on May 14, 2003 under 37 CFR 1.131 is sufficient to overcome the Rumsey et al. (US 2003/0000738 A1) and Huang (US 2002/0096764 A1) references having filing dates of June 25, 2001 and January 19, 2001 respectively.

### Allowed Subject Matter

3. Claims 2 – 17, 19 – 28, 63 – 68, 70 – 73, 76 – 81 are allowed.

The following is an examiner's statement of reasons for allowance.

Sambucetti et al. (US 6,335,104) teaches (Figures 1 and 2, columns 5 – 7, lines 1 - 26) a method of preparing a copper bond pad (12) surface for electrical connection by either a wirebond or a solder bump. Sambucetti et al. teaches forming a shared metallurgy structure (10) of the same composition and structure by depositing a diffusion barrier (16) comprising of nickel over and in contact with the copper bond pad (12) and a passivation layer of gold (18) over and in contact with the nickel containing layer (16) for attaching a solder bump (40) or a wire bond (30).

Sambucetti et al. does not teach providing metallurgy structures which comprise of underbump metallurgy layers on the respective input/output pads, barrier layers on the underbump metallurgy lavers, and passivation layers on the barrier layers, wherein the applicant has defined in the specification, that the underbump metallurgy layer

comprises of a first adhesion layer such as titanium or tantalum and a second conduction layer comprised of gold or copper over the adhesion layer.

Claims 3 –12, 17, 19 – 28, 63, 70 -72, 78, 80

The prior art does not fairly teach or suggest in combination with the other claimed limitations, a method of providing underbump metallurgy layers on the respective input/output pads, barrier layers on the underbump metallurgy layers, and passivation layers on the barrier layers, wherein the underbump metallurgy layers consist of first adhesion layer and a second conduction layer over the adhesion layer.

Claims 2, 13 –16, 77

The prior art does not fairly teach or suggest in combination with the other claimed limitations, a method of providing metallurgy structures for input/output pads of an electronic device comprising a substrate including semiconductor portions thereof, and first and second input/output pads on the substrate, the method comprising: providing first and second metallurgy structures on the first and second input/output pads, the first and second metallurgy structures having a shared metallurgy structure adapted to receive solder and wire bonds wherein the electronic device further comprises a protective insulating layer on the substrate and on portions of the first and second input/output pads so that portions of the input/output pads are exposed through the protective insulating layer.

Claims 64 – 68, 79, 81

The prior art does not fairly teach or suggest in combination with the other claimed limitations, a method for providing bonding structures for input/output pads of an electronic device comprising a substrate and first and second input/output pads on the substrate, the method comprising: providinq first and second barrier layers on the respective first and second input/output pads wherein the first and second barrier layers each comprise nickel wherein the first and second barrier layers have a same thickness; providing first and second passivation layers on the respective first and second barrier layers wherein the first and second passivation layers comprise a same material other than nickel and have a same thickness; providing a solder structure on the first passivation laver while maintaining the second passivation layer free of solder, and reflowing the solder structure so that the first passivation layer diffuses into the solder structure.

Claim 73

The prior art does not fairly teach or suggest in combination with the other claimed limitations, a method of forming an electronic device comprising:
forming first and second input/output pads on a substrate, forming a first bonding structure on the first input/output pad, the first bonding structure including a first barrier layer comprising nickel on the first input/output pad, and a solder structure on the first barrier layer; forming a second bonding structure on the second input/output pad, the second bonding structure including a second barrier layer comprising nickel on the second input/output pad and a gold layer on the second barrier layer comprising nickel;

bonding a wire to the second bonding structure, and bonding a second substrate to the solder structure so that the wire and the second substrate are bonded to the first substrate at a same time, wherein the first barrier layer comprises a nickel layer free of lead and an alloy layer including nickel and lead between the nickel layer free of lead and the solder structure.

Claims 76

The prior art does not fairly teach or suggest in combination with the other claimed limitations, a method of forming an electronic device comprising:

forming first and second input/output pads on a substrate, forming a protective insulating layer on the substrate and on portions of the first and second input/output pad pads so that portions of the first and second input/output pads are exposed through the protective insulating layer, forming a first bonding structure on the first input/output pad, the first bonding structure including a first barrier layer comprising nickel on the input/output pad, and a solder structure on the first barrier layer; forming a second bonding structure on the second input/output pad, the second bonding structure including a second barrier layer comprising nickel on the second input/output pad and a gold layer on the second barrier layer comprising nickel; bonding a wire to the second bonding structure and bonding a second substrate to the solder structure so that the wire and the second substrate are bonded to the first substrate at a same time.

***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Elenius et al. (US 2001/0011764 A1) teaches a chip scale package using large ductile solder balls.

Danziger et al. (US 6,221,682) teaches a method and apparatus for forming interconnects.

Degani et al. (EP 0782191 A2) teaches a multi-level stacked integrated circuit chip assembly.

Jao (US 6,415,974 B2) teaches a structure with solderbumps with improved coplanarity.

Chiang (US 2002/0086520) teaches a semiconductor device having a bump electrode.

Yung (US 5,162,257) teaches a solder bump fabrication method.

Ma (US 6,208,018 B1) teaches a piggyback multiple dice assembly.

Merrill et al. (US 5,886,393) teaches a bonding wire inductorfor use in an integrated circuit.

Mis (US 5,902,686) teaches methods for forming an inter-metallic region between a solder bump and a under-bump metallurgy region.

Kuo (US 2002/0197842 A1) teaches a solder bump process using a solder reservoir.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William C. Vesperman whose telephone number is 571-272-1701. The examiner can normally be reached on Mon. - Fri., 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl White, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WCV

wcv

Art Unit 2813

March 15, 2004

C. Chaudhari

**Chandra Chaudhari**
**Primary Examiner**